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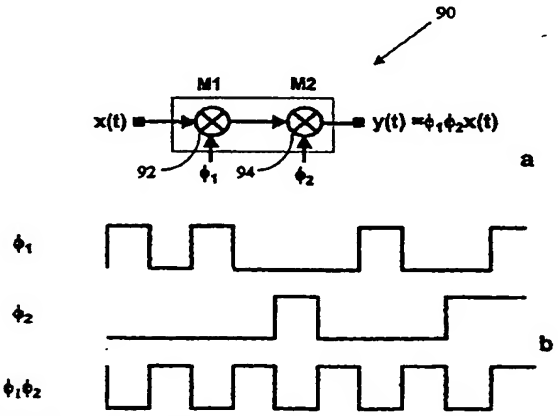
(54) Title: IMPROVED METHOD AND APPARATUS FOR UP-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS



(57) Abstract: This patent describes a method and system which overcomes the LO-leakage problem of direct conversion and similar RF transmitters. To solve this problem a virtual LO™ signal is generated within the baseband which is tuned to the incoming RF signal. The virtual local oscillator (VLO) signal is constructed using signals that do not contain a significant amount of power (or no power at all) at the wanted output RF frequency. Any errors in generating the virtual LO signal are minimized using a closed loop correction scheme.

WO 01/17121 A1

Improved Method and Apparatus for Up-Conversion of Radio Frequency (RF) Signals

The present invention relates generally to communications, and more specifically, to a fully-integrable method and apparatus for up-conversion of radio frequency (RF) and baseband signals with reduced local oscillator (LO) leakage.

Background of the Invention

Many communication systems modulate electromagnetic signals from baseband to higher frequencies for transmission, and subsequently demodulate those high frequencies back to their original frequency band when they reach the receiver. The original (or baseband) signal, may be, for example: data, voice or video. These baseband signals may be produced by transducers such as microphones or video cameras, be computer generated, or transferred from an electronic storage device. In general, the high transmission frequencies provide longer range and higher capacity channels than baseband signals, and because high frequency RF signals can propagate through the air, they can be used for wireless channels as well as hard wired or fibre channels.

All of these signals are generally referred to as radio frequency (RF) signals, which are electromagnetic signals, that is, waveforms with electrical and magnetic properties within the electromagnetic spectrum normally associated with radio wave propagation. The electromagnetic spectrum was traditionally divided into 26 alphabetically designated bands, however, the ITU formally recognizes 12 bands, from 30 Hz to 3000 GHz. New bands, from 3 THz to 3000 THz, are under active consideration for recognition.

Wired communication systems which employ such modulation and demodulation techniques include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet. These networks generally communication data signals over electrical or optical fibre chanels. Wireless communication systems which may employ modulation and demodulation include those for public broadcasting such as AM and FM radio, and UHF and VHF television. Private communication systems may include cellular telephone networks, personal paging devices, HF radio systems used by taxi services, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications. Other wired and

wireless systems which use RF modulation and demodulation would be known to those skilled in the art.

One of the current problems in the art, is to develop physically small and inexpensive modulation techniques and devices that have good performance characteristics. For cellular telephones, for example, it is desirable to have a transmitter which can be fully integrated onto an integrated circuit.

Several attempts have been made at completely integrating communication transmitter designs, but have met with limited degrees of success. Existing solutions and their associated problems and limitations are summarized below:

1. Direct Conversion Transmitter

Direct conversion architectures **10** modulate baseband signals to RF levels in a single step by mixing a baseband signal with a local oscillator signal at the carrier frequency. Referring to the block diagram of **Figure 1**, the in-phase (I) and quadrature (Q) components of the baseband signal are up-converted to RF via mixers MI **12** and MQ **14**, respectively. The RF mixing signals are generated using a local oscillator **16** tuned to the RF, and a 90 degree phase shifter **18** which ensures that the I and Q signals are up-converted into their quadrature components. The two up-converted RF signals are added together via the summing element S **20**, and filtered via a band pass filter (BPF) **22** having a pass band response around the RF signal to remove unwanted components. Finally, a power amplifier (PA) **26** amplifies the signal to the necessary transmission level.

Generally, a mixer is a circuit or device that accepts as its input two different frequencies and presents at its output:

(a) a signal equal in frequency to the sum of the frequencies of the input signals;

(b) a signal equal in frequency to the difference between the frequencies of the input signals; and

(c) the original input frequencies.

The typical embodiment of a mixer is a digital switch, which may generate significantly more tones than those shown above.

Hence, the disadvantages of this topology are:

- the LO signal leaks into the RF signal, since the RF output signal is at the same frequency as the LO signal; and
- the output RF signal leaks back into the LO generation elements, causing it to detune. This mechanism is commonly referred to "LO pulling".

However, this topology can easily be integrated and requires fewer components than other modulation topologies known in the art.

2. Directly Modulated Transmitter

Figure 2 presents a block diagram of a directly modulated transmitter **30** in which the baseband signal modulates a voltage control oscillator (VCO) **32**, designed to oscillate within the vicinity of the RF frequency. The output of the VCO **32** is then filtered by a bandpass filter (BPF) **34** which has a pass band around the RF frequency to remove unwanted components. A power amplifier **36** then amplifies the filtered signal to the amplitude required.

The disadvantages of this topology are:

- the LO signal leaking into the RF signal; and
- the output RF signal leaking back into the LO generation element, causing it to detune. Again, this mechanism is commonly referred to "LO pulling".

This topology can easily be integrated and requires a small number of components. To maintain stability, the VCO **32** is locked via a phase lock loop in most applications. In some applications, the input to the VCO **32** could be an up-converted version of the baseband signal.

3. Dual Conversion Transmitter

A dual conversion topology solves two of the problems associated with the direct conversion and the direct modulation topologies, specifically, the LO signal leaking into the RF signal and "LO pulling". In this topology the baseband signal is translated to the RF band via two frequency translations, which are associated with two local oscillators (LOs), neither of which is tuned to the RF signal. Because neither of these LOs are tuned to the desired RF output frequency, the LO leakage problem and "LO pulling" problem are generally eliminated.

The dual conversion topology is presented as a block diagram in **Figure 3**. Like the direct conversion transmitter described with respect to **Figure 1** hereinabove, the in-phase (I) and quadrature (Q) components of the base-band signal are first up-converted to RF via the mixers MI **42** and MQ **44**, respectively. However, in this case, the RF mixing signal generated using local oscillator **46** is not tuned to the desired output frequency, but is tuned to an intermediate frequency (IF). The 90 degree phase shifter **48** then ensures that the I and Q signals are up-converted into their quadrature IF components. The two-upconverted IF signals are then added together via the summing element S **50**, and filtered via a band pass filter (BPF) **52** having a pass band response around the IF signal.

The IF signal is then up-converted to the desired RF output frequency via mixer M **54** and a second local oscillator (LO2) **55**, which need not be at the RF output frequency. The signal is then filtered via a second band pass filter (BPF) **56** having a pass band around the RF signal, and is amplified to the desired level using power amplifier (PA) **26**.

Though this technique addresses the problems with the direct conversion and the direct modulation topologies, it has disadvantages of its own:

- it requires two LO signals;
- it requires two filters;
- it requires a significant amount of frequency planning; and
- it is difficult to integrate all the components into an integrated circuit.

4. Offset Conversion Transmitter

An offset conversion topology **60** such as that presented in **Figure 4**, also solves the two main problems associated with direct conversion and direct modulation, that is, the LO signal leaking into the RF signal and "LO pulling". Like the dual conversion transmitter, this is done by translating the baseband signal to the RF band using two local oscillators, neither of which are tuned to the RF output frequency. As noted above, the LO leakage problem and "LO pulling" problem are avoided, because neither of these LOs are tuned to the RF output frequency.

Referring to the block diagram of **Figure 4**, the baseband signal is up-converted to the RF frequency via mixers MI **62** and MQ **64** which are modulated by a combined signal from two separate oscillators LO1 **66** and LO2 **68**. The frequency used to up-convert the base band signal is equal to f1 + f2 where f1 is the fundamental frequency component of the local oscillator LO1 **66** signal and f2 is the fundamental component of the local oscillator LO2 **68** signal. Mixing the signals from oscillators LO1 **66** and LO2 **68** via the mixer M **70** generates the frequency f1 + f2, which corresponds to the RF output frequency. A band pass filter (BPF) **72** is then used to attenuate all frequency components except f1 + f2. The 90 degree phase shifter **74** ensures the I and Q signals are up-converted into their quadrature components.

The two-upconverted signals are then added together via the summing element S **76**, and filtered via a band pass filter (BPF) **78** having a pass band around the RF signal. Finally, a power amplifier **80** amplifies the signal to the desired level.

The disadvantages of this topology are:

- it requires two LO signals;
- it requires two filters; and
- it requires a significant amount of frequency planning.

There is therefore a need for a method and apparatus of modulating RF signals which allows the desired integrability along with good performance.

Summary of the Invention

It is therefore an object of the invention to provide a novel method and system of modulation which obviates or mitigates at least one of the disadvantages of the prior art.

One aspect of the invention is broadly defined as a radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising: a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of the local oscillator signal being emulated; a first mixer coupled to the synthesizer for mixing the input signal *x(t)* with the time-varying signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and a second mixer coupled to the synthesizer and to the output of the first mixer for mixing the signal $x(t)\ \varphi_1$ with the time-varying signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

Brief Description of the Drawings

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings in which:

Figure 1 presents a block diagram of a direct conversion transmitter as known in the art;

Figure 2 presents a block diagram of a directly modulated transmitter as known in the art;

Figure 3 presents a block diagram of a dual conversion transmitter as known in the art;

Figure 4 presents a block diagram of offset conversion transmitter as known in the art;

Figure 5 (a) presents a block diagram of a broad implementation of the invention;

Figure 5 (b) presents exemplary mixer input signals functions φ_1 and φ_2 plotted in amplitude against time;

Figure 6 presents a block diagram of quadrature modulation in an embodiment of the invention;

Figure 7 presents a block diagram of an embodiment of the invention employing error correction by measuring the amount of power at baseband;

Figure 8 presents a block diagram of a transmitter in a preferred embodiment of the invention;

Figure 9 presents a block diagram of an embodiment of the invention employing a filter placed between mixers M1 and M2; and

Figure 10 presents a block diagram of an embodiment of the invention employing N mixers and N mixing signals.

Detailed Description of Preferred Embodiments of the Invention

A device which addresses the objects outlined above, is presented as a block diagram in **Figure 5(a)**. This figure presents a modulator topography **90** in which an input signal *x(t)* is mixed with signals which are irregular in the time domain (TD), which effect the desired modulation. A virtual local oscillator (VLO) is generated by multiplying two functions (labelled φ_1 and φ_2) within the signal path of the input signal *x(t)* using two mixers M1 **92** and M2 **94**. The mixers described within this invention would have the typical properties of mixers within the art, that is, they would have an associated noise figure, linearity response, and conversion gain. The selection and design of these mixers would follow the standards known in the art, and could be, for example, double balanced mixers. Though this figure implies various elements are implemented in analogue form they can be implemented in digital form.

The two time-varying functions φ_1 and φ_2 that comprise the virtual local oscillator (VLO) signal have the property that their product emulates a local oscillator (LO) signal that has significant power at the carrier frequency, but neither of the two signals has a significant level of power at the frequency of the local oscillator being emulated. As a result, the desired modulation is affected, but there is no LO signal to leak in the RF path. **Figure 5b** depicts possible functions for φ_1 and φ_2.

To minimize the leakage of LO power into the RF output signal, as in the case of direct conversion and directly modulated topologies, the preferred criteria for selecting the functions φ_1 and φ_2 are:

(i) that φ_1 and φ_2 do not have any significant amount of power at the output frequency. That is, the amount of power generated at the output frequency should not effect the overall system performance of the transmitter in a significant manner;

(ii) the signals required to generate φ_1 and φ_2 should not have a significant amount of power at the output frequency; and

(iii) if x(t) is a baseband signal, $\varphi_1 * \varphi_1 * \varphi_2$ and $\varphi_2 * \varphi_2$ should not have a significant amount of power within the bandwidth of the up-converted RF (output) signal.

Conditions (i) and (ii) ensure an insignificant amount of power is generated within the system at the frequencies which would cause an equivalent LO leakage problem found in conventional direct conversion and directly modulated topologies. Condition (iii) ensures that if φ_1 leaks into the input port, it does not produce a signal within the RF signal at the output. Condition (iii) also ensures that if φ_2 leaks into node between the two mixers, it does not produce a signal within the RF signal at the output.

Various functions can satisfy the conditions provided above, several of which are described hereinafter, however it would be clear to one skilled in the art that other similar pairs of signals may also be generated. These signals can in general be random, pseudo-random, periodic functions of time, or digital waveforms. While these signals may be described as "aperiodic", groups of cycles may be repeated successively. For example, the φ_1 and φ_2 signals presented in **Figure 5(b)** which generate the five-cycle $\varphi_1 * \varphi_2$ signal, may be input to mixers M1 **92** and M2 **94** repeatedly.

As well, rather than employing two mixing signals shown above, sets of three or more signals may be used (additional description of this is given hereinafter with respect to **Figure 10**).

It would also be clear to one skilled in the art that virtual LO signals may be generated which provide the benefits of the invention to greater or lesser degrees. While it is possible in certain circumstances to have almost no LO leakage, it may be acceptable in other circumstances to incorporate apply virtual LO signals which still allow a degree of LO leakage.

The topology of the invention is similar to that of direct up-conversion, but provides a fundamental advantage: minimal leakage of a local oscillator (LO) signal into the RF band. The topology also provides technical advantages over other known topologies such as directly modulated, dual conversion and offset conversion transmitters:

- removes the necessity of having a second LO and various (often external) filters; and
- has a higher level of integration as the components it does require are easily placed on an integrated circuit.

While the basic implementation of the invention may produce errors in generating the virtual local oscillator (VLO), solutions to this problem are available and are described hereinafter.

The invention provides the basis for a fully integrated communications transmitter. Increasing levels of integration have been the driving impetus towards lower cost, higher volume, higher reliability and lower power consumer electronics since the inception of the integrated circuit. This invention will enable communications transmitters to follow the same integration route that other consumer electronic products have benefited from.

Specifically, advantages from the perspective of the manufacturers when incorporating the invention into a product include:

1. significant cost savings due to the decreased parts count of an integral device. Decreasing the parts count reduces the cost of inventory control, reduces the costs associated with warehousing components, and reduces the amount of manpower to deal with higher part counts;
2. significant cost savings due to the decreased manufacturing complexity. Reducing the complexity reduces time to market, cost of equipment to manufacture the product, cost of testing and correcting defects, and reduces time delays due to errors and problems on the assembly line;
3. reduces design costs due to the simplified architecture. The simplified architecture will shorten the first-pass design time and total design cycle time as a simplified design will reduce the number of design iterations required;
4. significant space savings and increased manufacturability due to the high integrability and resulting reduction in product form factor (physical size). This implies huge savings throughout the manufacturing process as smaller device footprints enable manufacturing of products with less material such as

printed circuit substrate, smaller product casing and smaller final product packaging;

5. simplification and integrability of the invention will yield products with higher reliability, greater yield, less complexity, higher life span and greater robustness;

6. due to the aforementioned cost savings, the invention will enable the creation of products that would otherwise be economically unfeasible;

Hence, the invention provides the manufacturer with a significant competitive advantage.

From the perspective of the consumer, the marketable advantages of the invention include:

1. lower cost products, due to the lower cost of manufacturing;
2. higher reliability as higher integration levels and lower parts counts imply products will be less prone to damage from shock, vibration and mechanical stress;
3. higher integration levels and lower parts counts imply longer product life span;
4. lower power requirements and therefore lower operating costs;
5. higher integration levels and lower parts counts imply lighter weight products;
6. higher integration levels and lower parts counts imply physically smaller products; and
7. the creation of economical new products.

The present invention relates to the translation of a baseband signal directly to an RF signal and is particular concerned with solving the LO-leakage problem associated with the present art. The invention allows one to fully integrate a RF transmitter on a single chip without using external filters, while furthermore, the RF transmitter can be used as a multi-standard transmitter. Descriptions of exemplary embodiments follow.

In many modulation schemes, it is necessary to modulate both I and Q components of the input signal, which requires a modulator **100** as presented in the block diagram of **Figure 6**. In this case, four modulation functions would have to be generated: $\varphi_{1I} * \varphi_{2I}$ which is 90 degrees out of phase with $\varphi_{1Q} * \varphi_{2Q}$. The pairing of signals φ_{1I} and φ_{2I} must meet the function selection criteria listed above, as must the signal pairing of φ_{1Q} and φ_{2Q}. The mixers **102**, **104**, **106**, **108** are standard mixers as known in the art.

As shown in **Figure 6**, mixer **102** receives the input signal *x(t)* and modulates it with φ_{1I}; subsequent to this, mixer **104** modulates signal *x(t)* φ_{1I} with φ_{2I} to yield the in-phase component of the input signal at baseband, that is, *x(t)* $\varphi_{1I}\varphi_{2I}$. A complementary process occurs on the quadrature side of the modulator, where mixer **106** receives the input signal *x(t)* and modulates it with φ_{1Q}; after which mixer **108** modulates signal *x(t)* φ_{1Q} with φ_{2Q} to yield the quadrature phase component of the input signal at baseband, that is, *x(t)* $\varphi_{1Q}\varphi_{2Q}$. The in-phase and quadrature components of the up-converted signal are then combined using summer **110** to yield the output signal: *x(t)* $\varphi_{1I}\varphi_{2I}$ + *x(t)* $\varphi_{1Q}\varphi_{2Q}$.

In the analysis above timing errors that would arise when constructing the *VLO* have been neglected (timing errors can be in the form of a delay or a mismatch in rise/fall times). In the analysis which follows, only delays are considered, but the same analysis can be applied to rise/fall times. The actual *VLO* that is generated can be written as:

$$VLO_a = VLO_i + \varepsilon_{VLO}(t) \qquad (1)$$

where VLO_a is the actual *VLO* generated, VLO_i is the ideal *VLO* without any timing error, and $\varepsilon_{VLO}(t)$ absorbs the error due to timing errors. Therefore, the output signal of the virtual LO topology, denoted as y(t), becomes:

$$y(t) = x(t) \times [VLO_i + \varepsilon_{VLO}(t)] \qquad (2)$$

The term *x(t) VLOi* is the wanted term and *x(t)* $\varepsilon_{VLO}(t)$ is a term that could produce aliasing power into the wanted RF signal at the output of the structure. The term $\varepsilon_{VLO}(t)$ can also be thought of a term that raises the noise floor of the *VLO*. This is not that serious a problem because the signal *x(t)* is at baseband and has a well defined bandwidth. By selecting φ_1 and φ_2 carefully and by placing an appropriate filter at the input of the structure, the amount of aliasing power can be reduced significantly, though it can never be completely eliminated due to timing errors.

There are several ways one could further reduce the amount of aliasing power, for example, by using a closed loop configuration as described below. The term *x(t)* $\varepsilon_{VLO}(t)$ contains two terms at the RF output:

(i) aliasing power P_a, and

(ii) power of the wanted signal, but at a reduced power level which is on the order of delay error P_{we}

Therefore, the total power at the RF output (denoted by P_M) can be decomposed into three components:

(i) the power of the wanted RF signal, P_w,

(ii) the power of the aliasing terms, P_a, and

(iii) the power of the wanted RF signal arising from the term, $P_{w\varepsilon}$ (this power can either be positive or negative). Therefore,

$$P_M = P_w + P_{w\varepsilon}(\tau) + P_a(\tau) \qquad (3)$$

Note that $P_{w\varepsilon}$ and P_a are a function of the delay τ. Since $|P_w| >> |P_{w\varepsilon}|$, (3) becomes,

$$P_M = P_w + P_a(\tau) \qquad (4)$$

If the power, P_M is measured and τ is adjusted in time, one can reduce the term Pa to zero (or close to zero). Mathematically this can be done if the slope of P_M with the delay τ is set to zero; that is:

$$\frac{dP_M}{d\tau} = \frac{dP_a(\tau)}{d\tau} = 0 \qquad (5)$$

A transmitter **120** for implementing this procedure is illustrated in **Figure 7** (a more detailed description is provided in the paragraph below). The power measurement scheme and the element blocks required to detect when $\frac{dP_M}{d\tau} = 0$, can be implemented within a digital signal processing unit (DSP). Also illustrated in **Figure 7** is a visual representation of the power measured versus delay, which identifies an optimum point at which $\frac{dP_M}{d\tau} = 0$.

In the block diagram of **Figure 7** the baseband signal is first multiplied by the signals φ_1 and φ_2 via mixers M1 **122** and M2 **124**, respectively. The signal is next filtered via a band pass filter (BPF) **126**, which is used to reduce the amount of out-of-band power, which may cause the subsequent elements to compress in gain or distort the wanted signal. The design of this BPF **126** depends on the bandwidth of the wanted signal, the system specifications and system design trade offs. In the interest of simplicity, separate in-phase and quadrature channels have not been identified, though the invention is preferably implement as such.

The output of the BPF **126** is the desired up-converted RF signal. This output signal is measured with power measurement unit **128**. The power is minimized with respect to the delay added onto the signal φ_2 by use of

the $\frac{dP_M}{d(delay)} = 0$ detector **130**, and the delay controller **132** which manipulates the φ_2 signal source **134**. As shown in the timing diagram of **Figure 7**, this process allows signal φ_2 to be delayed in time.

In general, the power can be minimized with respect to the rise time of φ_2 or a combination of delay and rise time. Furthermore, the power can be minimized with respect to the delay, rise time, or both delay and rise time of the signal φ_1, or both φ_1 and φ_2. It would be clear to one skilled in the art that current or voltage may be measured rather than power in certain applications. As well, the phase delay of either or both of φ_1 and φ_2 may be modified to minimized the error.

It is preferred that this power detection **130** be done within a digital signal processing unit (DSP) **136** after the baseband signal is digitized via an analog to digital converter, but it may be done with separate components, or analogue components.

A problem that may prove to be more serious than aliasing power at the output, is a direct current offset accompanying the signal baseband signal *x(t)*. Letting *DC* represent the value of this unknown direct current offset, the input can be written as *x(t)* + *DC*. Therefore, the output of the structure would be of the form:

$$y(t) = x(t) \times [VLO_i] + DC \times VLO_i \qquad (6)$$

assuming there is no error associated with the generation of the *VLO* signal. In this presentation, the term $DC \times VLO_i$ represents unwanted power near the wanted signal $x(t) \times VLO_i$.

One method that can be used to remove this unwanted power, $DC \times VLO_i$, is to remove the DC offset using a calibration routing as presented in **Figure 8**. Briefly, the calibration routing of this transmitter **120** first sets the baseband signal to zero, then measures the output power, minimizing it against a parameter that adds an additional DC offset to the input of the structure via a summing device. The power measured can be made at any point after the two mixers, that is, it could be made at the output of a power amplifier driving the antenna.

Specifically, **Figure 8** presents a block diagram of a transmitter which produces a filtered and amplified baseband signal in generally the same manner as that of **Figure 7**. Hence, components **122**, **124** and **126** of **Figure 7** correspond with

components **142**, **144** and **146** of **Figure 8** respectively, though their input signals are slightly different.

It is preferred to generate the inputs to the two mixers **142** and **144** by means of signal generation blocks **148** and **150**; signal generation block **148** generating the φ_1 signal and signal generation block **150** generating the φ_2 signal. Implementing the invention with separate I and Q channels would require four mixers, two per channel, and four φ signals; specifically, $\varphi_1 I$ and $\varphi_1 Q$; and $\varphi_2 I$ and $\varphi_2 Q$, as shown in **Figure 6**.

The input to these generation blocks **148** and **150** is an oscillator which does not have a significant amount of signal power at the frequency of the desired output RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 5**. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. _____.

The embodiment of **Figure 8** is distinct from that of **Figure 7** with regard to the feedback control loop. Power measurement of the RF output signal is performed by the power measurement unit **152**, but rather than optimising for $\frac{dP_M}{d(delay)} = 0$ as per the embodiment presented in **Figure 7**, the control loop is optimised for - $\frac{dP_M}{d(DCoffset)} = 0$ using detector **154**, which drives the DC offset generator **156**.

DC offset is affected in the baseband signal by means of the summer **158** which sums the input baseband signal with the direct current offset from the DC offset generator **156**. Suitable components for the DC offset generator **156** and summer **158** are known in the art.

The physical order (that is, arrangement) of the BPF **146**, the DC offset correction summer **158**, and any additional gain control elements (none shown) can be rearranged to some degree. Such modifications would be clear to one skilled in the art.

As in the case of **Figure 7**, separate in-phase and quadrature channels have not been identified in the interest of simplicity, though the invention of **Figure 8** is preferably implement as such. As well, though the figure implies the use of analogue components, they can be implemented in digital form.

Also as in the case of **Figure 7**, it is preferred that the detector **154**, be embodied in a digital signal processor (DSP) **160**.

It would be clear to one skilled in the art that many variations may be made to the designs presented herein, without departing from the spirit of the invention. One such variation to the basic structure in **Figure 5a** is to add a filter **170** between the two mixers **92** and **94** as shown in the block diagram of **Figure 9** to remove unwanted signals that are transferred to the output port. This filter **170** may be a low pass, high pass, or band pass filter depending on the transmitter requirements. The filter **170** does not necessarily have to be a purely passive filter, that is, it can have active components.

Another variation is that several functions φ_1, φ_2, φ_3 ... φ_n may be used to generate the virtual LO, as presented in the block diagram of **Figure 10**. Here, φ_1* φ_2*... *φ_n has a significant power level at the LO frequency, but each of the functions φ_1... φ_n contain an insignificant power level at LO.

The electrical circuits of the invention may be described by computer software code in a simulation language, or hardware development language used to fabricate integrated circuits. This computer software code may be stored in a variety of formats on various electronic memory media including computer diskettes, CD-ROM, Random Access Memory (RAM) and Read Only Memory (ROM). As well, electronic signals representing such computer software code may also be transmitted via a communication network.

Clearly, such computer software code may also be integrated with the code of other programs, implemented as a core or subroutine by external program calls, or by other techniques known in the art.

The embodiments of the invention may be implemented on various families of integrated circuit technologies using digital signal processors (DSPs), microcontrollers, microprocessors, field programmable gate arrays (FPGAs), or discrete components. Such implementations would be clear to one skilled in the art.

The invention may be applied to various communication protocols and formats including: amplitude modulation (AM), frequency modulation (FM), frequency shift keying (FSK), phase shift keying (PSK), cellular telephone systems including

analogue and digital systems such as code division multiple access (CDMA), time division multiple access (TDMA) and frequency division multiple access (FDMA).

The invention may be applied to such applications as wired communication systems include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet, using electrical or optical fibre cable systems. As well, wireless communication systems may include those for public broadcasting such as AM and FM radio, and UHF and VHF television; or those for private communication such as cellular telephones, personal paging devices, wireless local loops, monitoring of homes by utility companies, cordless telephones including the digital cordless European telecommunication (DECT) standard, mobile radio systems, GSM and AMPS cellular telephones, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications.

While particular embodiments of the present invention have been shown and described, it is clear that changes and modifications may be made to such embodiments without departing from the true scope and spirit of the invention.

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said time-varying signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said time-varying signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1\ \varphi_2$; and

a time-varying signal modification circuit for modifying a parameter of one of said time-varying signals to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said time-varying signals.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said time-varying signals.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said time-varying signals.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where said time-varying signals can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, further comprising:
a filter for removing unwanted signal components from said $x(t)\ \varphi_1$ signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are irregular.

23. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:
a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said time-varying signals to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, further comprising:

a filter for removing unwanted signal components.

30. The radio frequency (RF) up-convertor of claim 1, further comprising:

a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

31. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal $x(t)$ with said time-varying signal φ_1 to generate an output signal $x(t)$ φ_1; and

mixing said signal $x(t)$ φ_1 with said time-varying signal φ_2 to generate an output signal $x(t)$ φ_1 φ_2.

32. An integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 30.

33. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 30.

34. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development

language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 30.

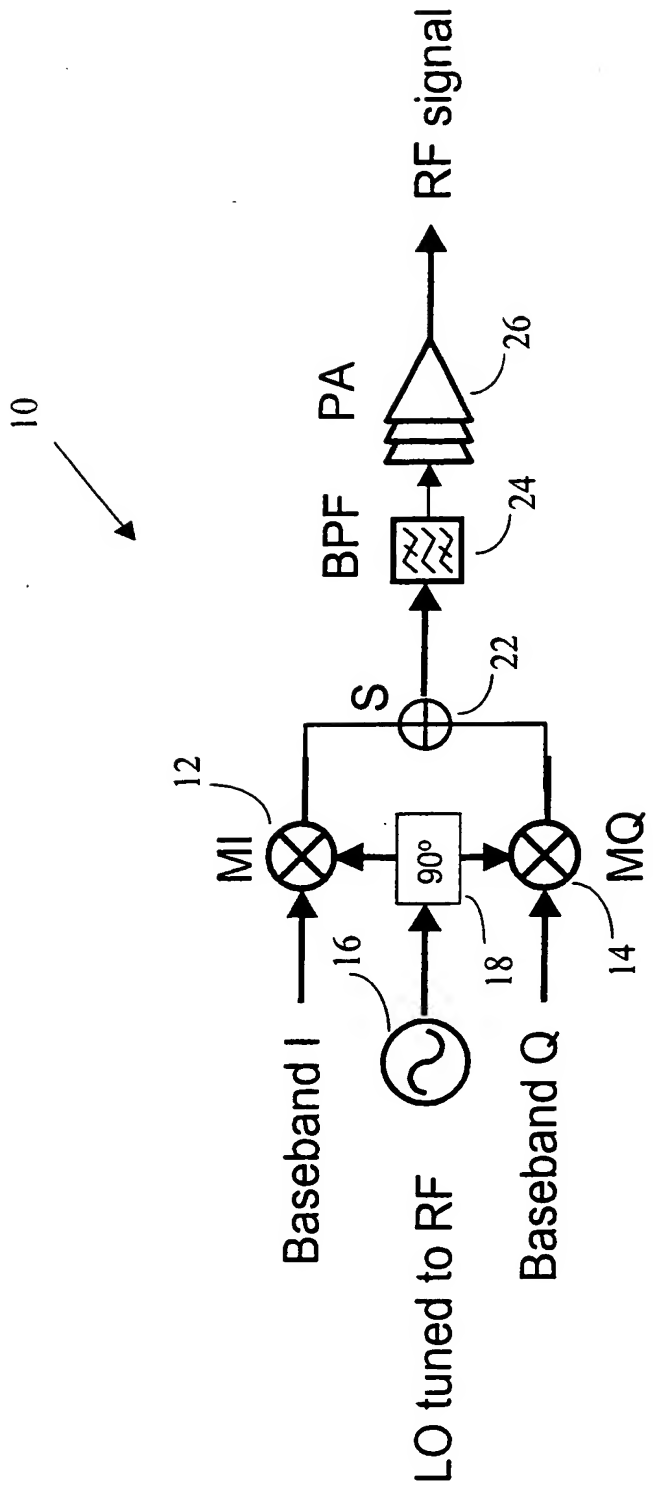


FIGURE 1 - PRIOR ART

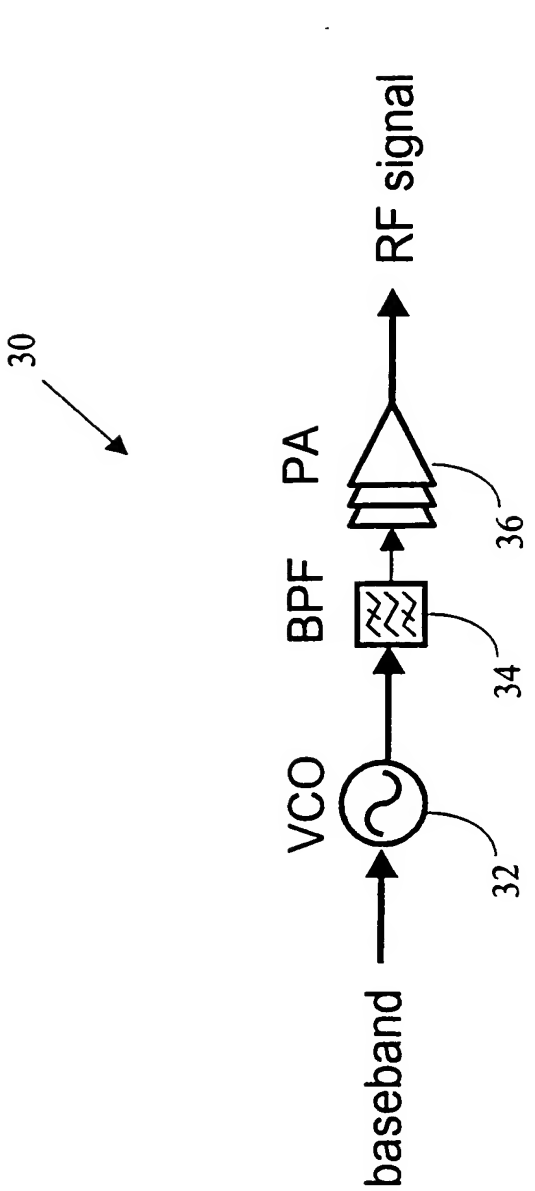


FIGURE 2 - PRIOR ART

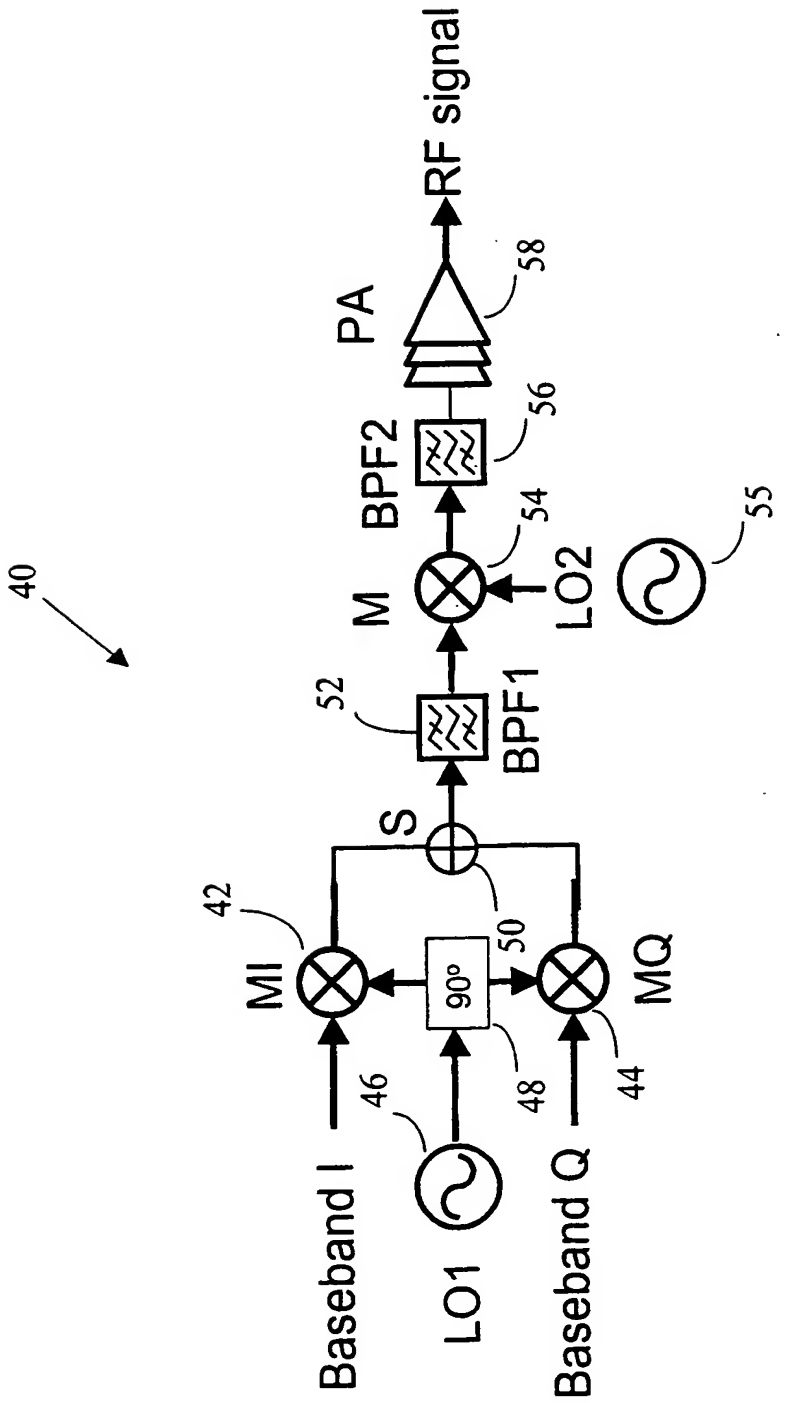


FIGURE 3 - PRIOR ART

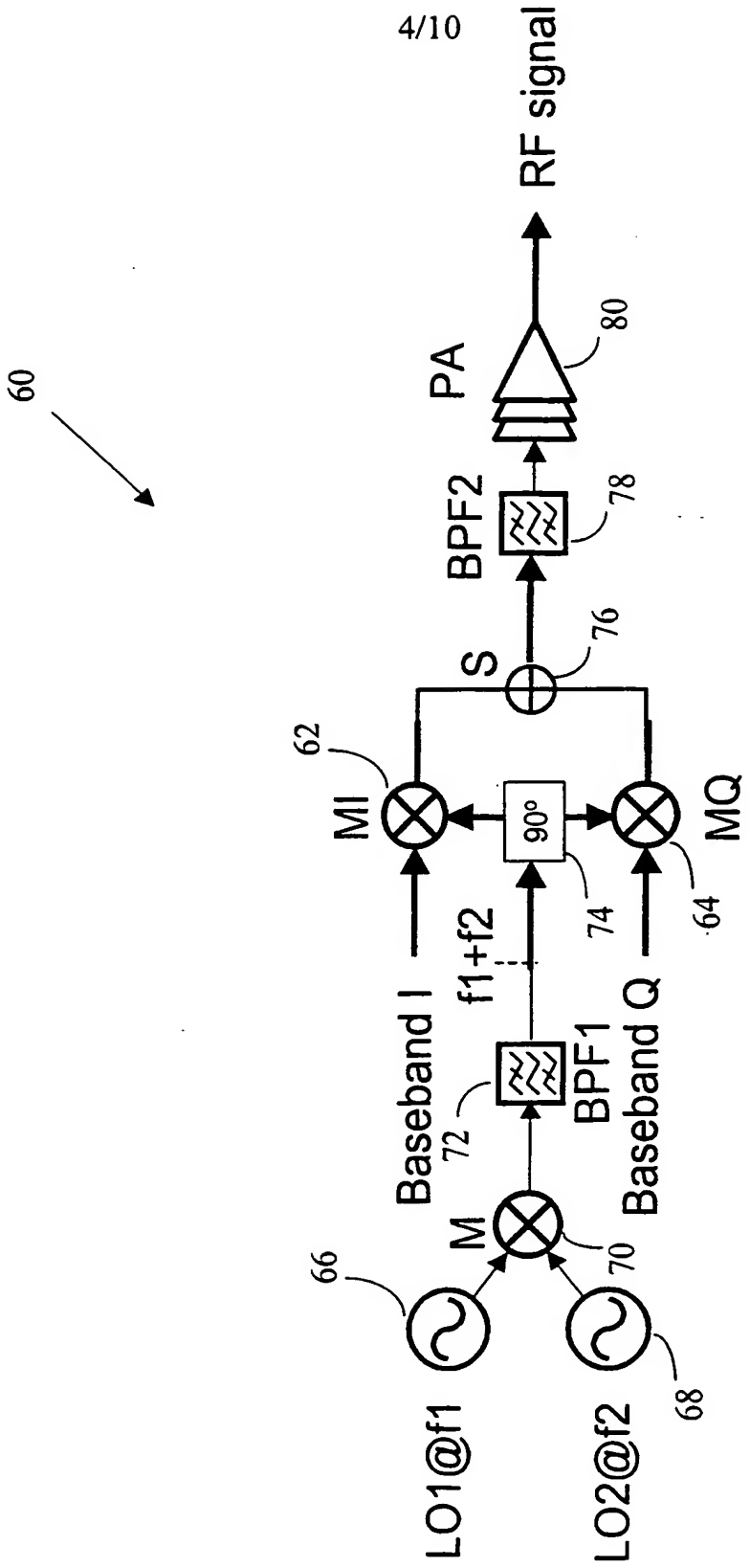


FIGURE 4 - PRIOR ART

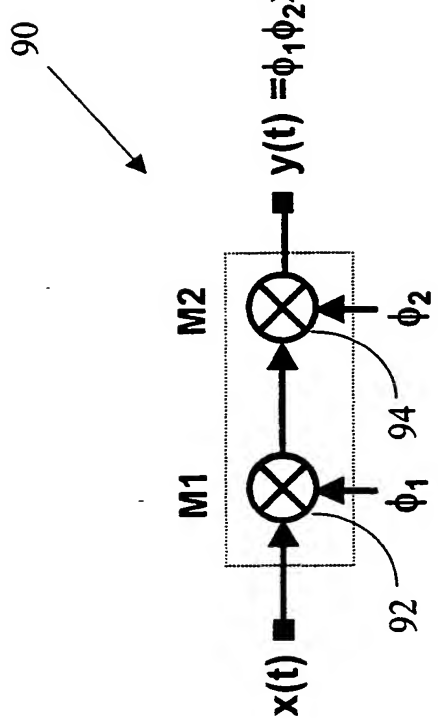


FIGURE 5(a)

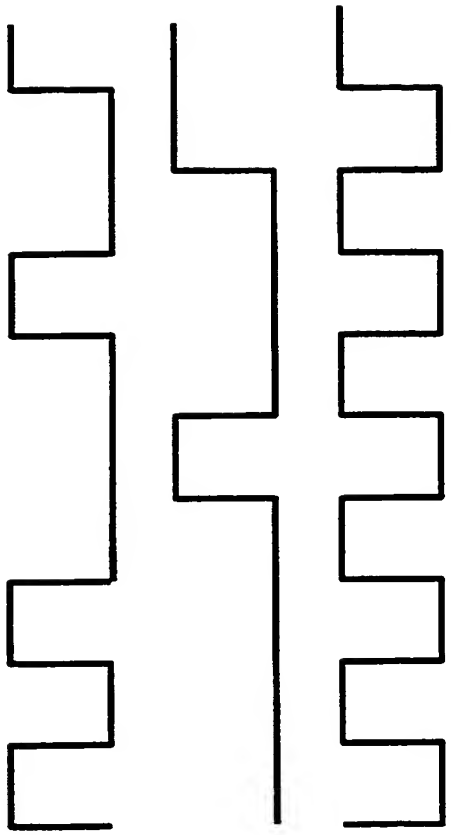


FIGURE 5(b)

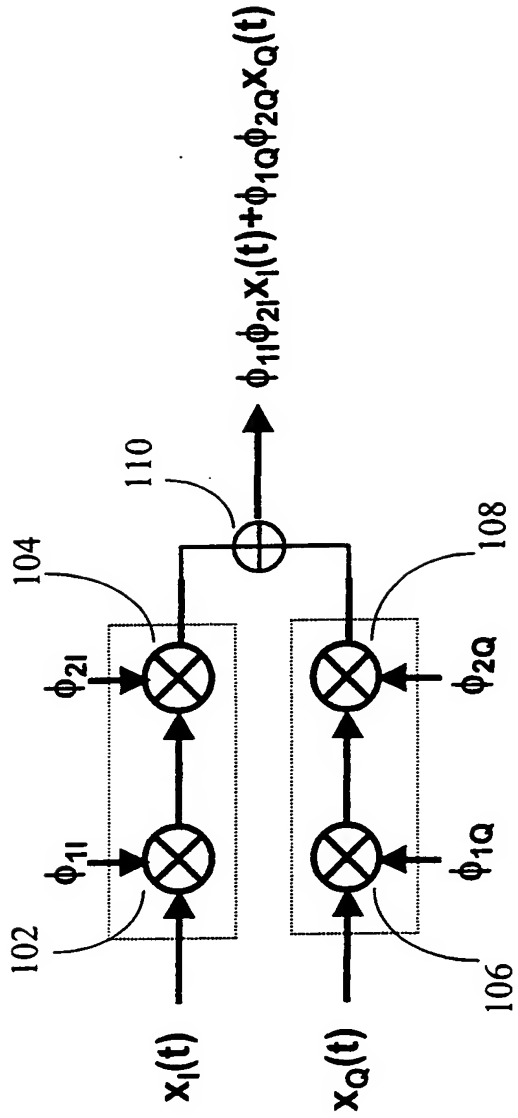

$\phi_{11}\phi_{21}x_I(t)+\phi_{1Q}\phi_{2Q}x_Q(t)$
110
104
108
ϕ_{21}
ϕ_{2Q}
ϕ_{11}
ϕ_{1Q}
102
106
$x_I(t)$
$x_Q(t)$
100

FIGURE 6

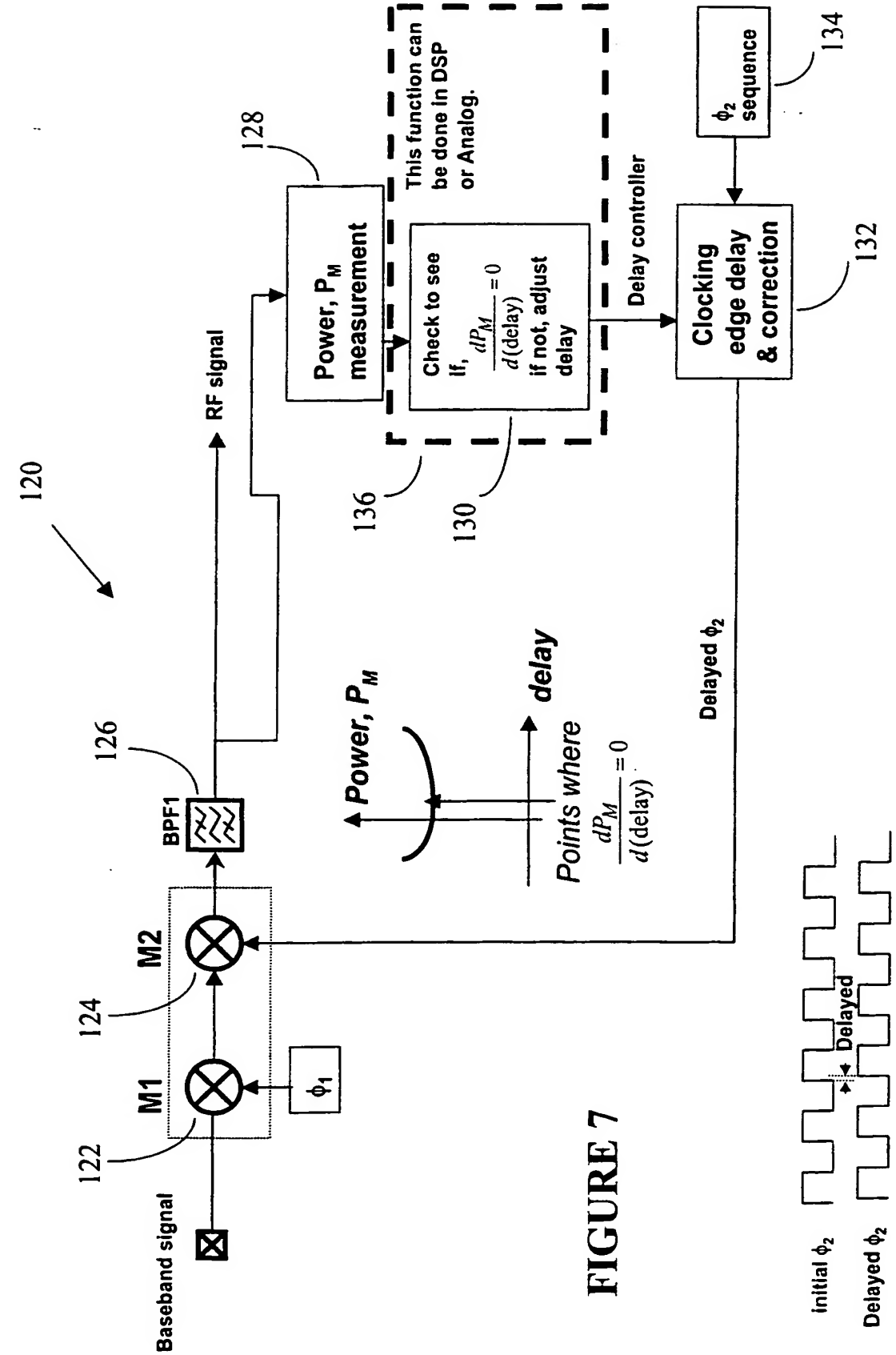

120
Baseband signal
122
M1
124
M2
126
BPF1
RF signal
128
Power, P_M measurement
This function can be done in DSP or Analog.
Check to see if, $\frac{dP_M}{d(\text{delay})} = 0$ if not, adjust delay
130
136
Delay controller
ϕ_1
ϕ_2 sequence
134
Clocking edge delay & correction
132
Delayed ϕ_2
Power, P_M
delay
Points where $\frac{dP_M}{d(\text{delay})} = 0$
Initial ϕ_2
Delayed
Delayed ϕ_2

FIGURE 7

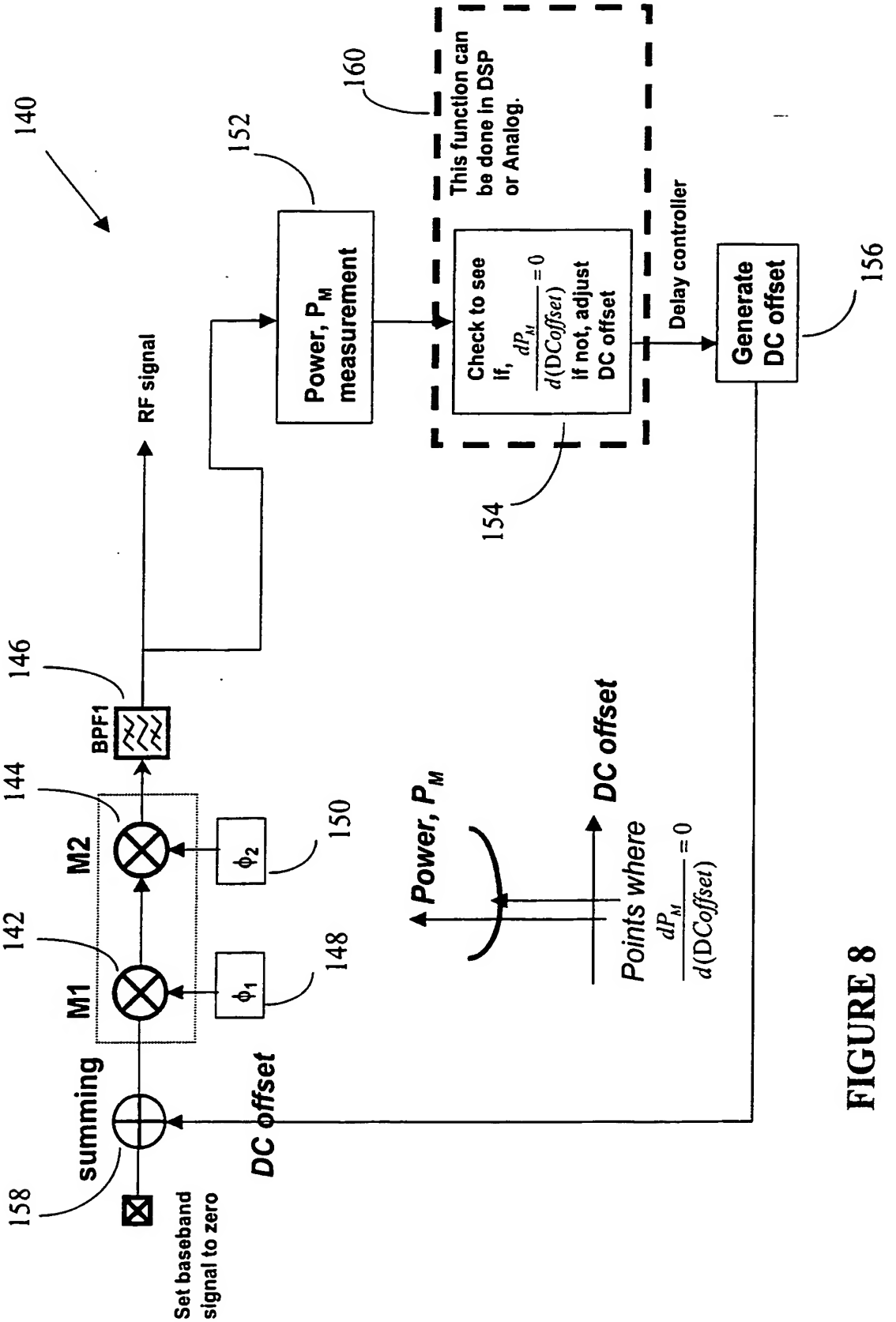

140
152
160
This function can be done in DSP or Analog.
Power, P_M measurement
Check to see if, $\frac{dP_M}{d(DCoffset)} = 0$ if not, adjust DC offset
Delay controller
Generate DC offset
156
154
RF signal
146
BPF1
144
M2
150
ϕ_2
142
M1
148
ϕ_1
summing
158
DC offset
Set baseband signal to zero
Power, P_M
DC offset
Points where $\frac{dP_M}{d(DCoffset)} = 0$

FIGURE 8

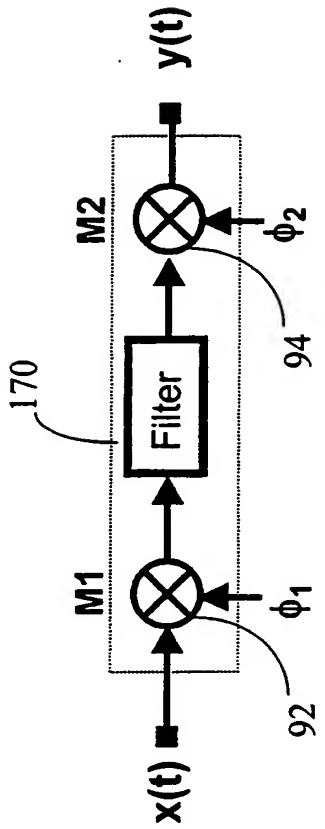


FIGURE 9

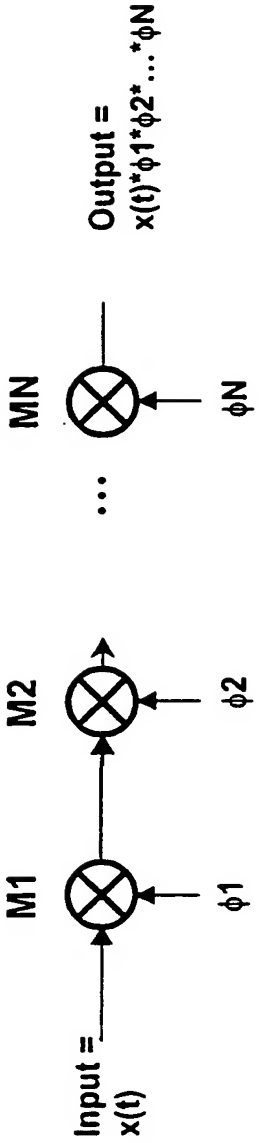


FIGURE 10

INTERNATIONAL SEARCH REPORT

Inte onal Application No
P[illegible]/CA 00/00995

A. CLASSIFICATION OF SUBJECT MATT
IPC 7 H04B1/04 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11) abstract page 2, line 1 - line 16 page 4, line 5 - line 22 claims 1-7; figure 2	1-3, 20-24, 29-31
X	EP 0 899 868 A (MITEL CORP) 3 March 1999 (1999-03-03) abstract column 1, line 22 - line 42 claims 1-6	1,20,21, 31

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2001	24/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Lazaridis, P

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte[redacted]onal Application No
PC[redacted]A 00/00995

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9601006 A	11-01-1996	AU 2909795 A	25-01-1996
EP 0899868 A	03-03-1999	CA 2245958 A	28-02-1999

components **142**, **144** and **146** of **Figure 8** respectively, though their input signals are slightly different.

It is preferred to generate the inputs to the two mixers **142** and **144** by means of signal generation blocks **148** and **150**; signal generation block **148** generating the φ_1 signal and signal generation block **150** generating the φ_2 signal. Implementing the invention with separate I and Q channels would require four mixers, two per channel, and four φ signals; specifically, $\varphi_1 I$ and $\varphi_1 Q$; and $\varphi_2 I$ and $\varphi_2 Q$, as shown in **Figure 6.**

The input to these generation blocks **148** and **150** is an oscillator which does not have a significant amount of signal power at the frequency of the desired output RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 5.** Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. _____.

The embodiment of **Figure 8** is distinct from that of **Figure 7** with regard to the feedback control loop. Power measurement of the RF output signal is performed by the power measurement unit **152**, but rather than optimising for $\frac{dP_M}{d(delay)} = 0$ as per the embodiment presented in **Figure 7**, the control loop is optimised for - $\frac{dP_M}{d(DCoffset)} = 0$ using detector **154**, which drives the DC offset generator **156.**

DC offset is affected in the baseband signal by means of the summer **158** which sums the input baseband signal with the direct current offset from the DC offset generator **156.** Suitable components for the DC offset generator **156** and summer **158** are known in the art.

The physical order (that is, arrangement) of the BPF **146**, the DC offset correction summer **158**, and any additional gain control elements (none shown) can be rearranged to some degree. Such modifications would be clear to one skilled in the art.

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said time-varying signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said time-varying signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1\ \varphi_2$; and

a time-varying signal modification circuit for modifying a parameter of one of said time-varying signals to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said time-varying signals.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said time-varying signals.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said time-varying signals.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where said time-varying signals can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, further comprising:
a filter for removing unwanted signal components from said $x(t)\ \varphi_1$ signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are irregular.

23. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said time-varying signals are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:
a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said time-varying signals to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, further comprising:

a filter for removing unwanted signal components.

30. The radio frequency (RF) up-convertor of claim 1, further comprising:

a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

31. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal $x(t)$ with said time-varying signal φ_1 to generate an output signal $x(t)$ φ_1; and

mixing said signal $x(t)$ φ_1 with said time-varying signal φ_2 to generate an output signal $x(t)$ φ_1 φ_2.

32. An integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 30.

33. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 30.

34. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development

language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 30.

PATENT COOPERATION TREATY

PCT

REC'D 29 JAN 2002

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70) 12

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
O8-887953WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA00/00995	01/09/2000	01/09/1999

International Patent Classification (IPC) or national classification and IPC
H04B1/04

Applicant
SiRiFIC WIRELESS CORPORATION

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 6 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
29/03/2001	25.01.2002

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/CA00/00995

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

1-12,14,15	as originally filed			
13	as received on	17/12/2001	with letter of	17/12/2001

Claims, No.:

1-33	as received on	17/12/2001	with letter of	17/12/2001

Drawings, sheets:

1/10-10/10	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2-29,30-33
	No:	Claims	1,30
Inventive step (IS)	Yes:	Claims	
	No:	Claims	2-29,31-33
Industrial applicability (IA)	Yes:	Claims	1-33
	No:	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:

   D1: WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11)
   D2: EP-A-0 899 868 (MITEL CORP) 3 March 1999 (1999-03-03)

2. Document D1, see in particular the passages cited in the search report, discloses as in claim 1:

   a radio frequency (RF) up-convertor with reduced local oscillator leakage for modulating an input signal x(t)(i.e. 80 MHz, D1 clearly discloses that the convertor can be used for transmission conversion, see claim 11 and page 7 line 12, this implies an up-conversion, although the frequencies refer to the embodiment of Figure 2 which relates to a down-conversion), comprising:
   a synthesizer for generating mixing signals φ1 and φ2 which vary irregularly over time (because they are spread); where φ1*φ2 has significant power at the frequency (i.e. 81 MHz) of the local oscillator being emulated, and neither φ1 nor φ2 has significant power at the frequency of said local oscillator being emulated (even though the signals φ1 and φ2 are spread they do not have significant energy at 81 MHz)

   a first mixer (21) coupled to said synthesizer for mixing said input signal x(t) with said mixing signal φ1 to generate an output signal x(t) φ1 (any mixer generates an output signal composed from the product of its input signals); and

   a second mixer (26) coupled to said synthesizer and to the output of said first mixer for mixing said signal x(t) φ1 with said mixing signal φ2 to generate an output signal x(t) φ1 φ2. (again, a mixer generates an output signal composed from the product of its input signals).

   The references in parentheses apply to the figures of D1.

It should be noted that the structure claimed by claim 1 is identical to the structure disclosed by D1 in its claim 1 which does not provide any additional filters.

Since all the features of claim 1 are known from D1, the claim lacks novelty in the sense of Article 33(1),(2) PCT.

3. The subject-matter of independent claim 30 corresponds to the subject-matter of claim 1, hence the above argumentation correspondingly applies to independent method claim 30.

4. Dependent claims 2 to 29 and 31 to 33 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, involve an inventive step (Article 33(3) PCT) since these claims merely define an association of known features (see also D2 to D4) functioning in their normal way and, in combination, not producing any non-obvious working interrelationship, cf. PCT Guidelines Chapt. IV,8.8(B1).

Re Item VII

Certain defects in the international application

1. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D2 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII

Certain observations on the international application

1. Claim 1 tries to define the up-converter using parameters (the power at the frequency of a local oscillator being emulated) which are unsuitable to clearly define the structure of the up-convertor to be protected. Claim 1 is thus unclear in the sense of Article 6 PCT.

2. Claim 2 tries to define the convertor by reference to the input signal x(t) which may be applied to the a mixer of the convertor. Such a definition is unsuitable to clearly define the structure of the claimed convertor. This claims is thus unclear,

Article 6 PCT.

components **142**, **144** and **146** of **Figure 8** respectively, though their input signals are slightly different.

It is preferred to generate the inputs to the two mixers **142** and **144** by means of signal generation blocks **148** and **150**; signal generation block **148** generating the φ_1 signal and signal generation block **150** generating the φ_2 signal. Implementing the invention with separate I and Q channels would require four mixers, two per channel, and four φ signals; specifically, $\varphi_1 I$ and $\varphi_1 Q$; and $\varphi_2 I$ and $\varphi_2 Q$, as shown in **Figure 6**.

The input to these generation blocks **148** and **150** is an oscillator which does not have a significant amount of signal power at the frequency of the desired output RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 5**. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. PCT/CA00/00996.

The embodiment of **Figure 8** is distinct from that of **Figure 7** with regard to the feedback control loop. Power measurement of the RF output signal is performed by the power measurement unit **152**, but rather than optimising for $\frac{dP_M}{d(delay)} = 0$ as per the embodiment presented in **Figure 7**, the control loop is optimised for $\frac{dP_M}{d(DCoffset)} = 0$ using detector **154**, which drives the DC offset generator **156**.

DC offset is affected in the baseband signal by means of the summer **158** which sums the input baseband signal with the direct current offset from the DC offset generator **156**. Suitable components for the DC offset generator **156** and summer **158** are known in the art.

The physical order (that is, arrangement) of the BPF **146**, the DC offset correction summer **158**, and any additional gain control elements (none shown) can be rearranged to some degree. Such modifications would be clear to one skilled in the art.

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal *x(t)* φ_1; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal *x(t)* φ_1 with said mixing signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal *x(t)* φ_1 φ_2; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, where said filter comprises:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:
a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

30. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal $x(t)$ with said mixing signal φ_1 to generate an output signal $x(t)$ φ_1; and

mixing said signal $x(t)$ φ_1 with said mixing signal φ_2 to generate an output signal $x(t)$ φ_1 φ_2.

31. An integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

32. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

33. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

IN THE EUROPEAN PATENT OFFICE

The International Preliminary Examining Authority

In The Matter of International (PCT) Patent Application:

Applicant	: **SiRiFIC Wireless Corporation; et al.**
Serial No.	: **PCT/CA00/00995**
Filing Date	: **September 1, 2000**
Title	: **Improved Method And Apparatus For Up-Conversion Of Radio Frequency (RF) Signals**
Our File	: **08887953WO**
Date	: **December 17, 2001**

European Patent Office
Erhardstrasse 27
D-80298 Munich
FEDERAL REPUBLIC OF GERMANY

Response to Written Opinion

Dear Sir:

In response to the Written Opinion dated July 17, 2001, kindly amend this application as follows:

In the Description:

Substitute the attached page 13, for the corresponding page 13 presently on file.

In the Claims:

Substitute the attached claims pages 35 - 36, containing amended claims 12 - 21 for the corresponding pages 35 - 36 presently on file.

REMARKS

The Applicant notes that claims 1 and 31 have been amended, replacing the wording "time-varying" with "varying irregularly over time". The basis for this wording is found in the specification, particularly at lines 15 - 18 of page 6. Claims 22 and 29 have been amended and claim 30 has been deleted. The amended claim 22 has basis in the specification at lines 6 - 7 of page 8, and amended claim 29 has basis in Figure 5(b) and page of the description, at lines 20 - 27. Other small amendments have also been made to other claims.

A compare document identifying the amendments made to the claims, has been attached, deleted text being struck-through and new text being underlined. No new matter has been added by way of these amendments.

Page 13 of the specification has been amended to enter the serial no. of the co-pending patent application referred to in the subject patent application as originally filed.

Under item V. 2. of the Written Opinion, the Examiner rejected claim 1 as lacking novelty in view of the publication of patent application WO 96 01006 (the "Honeywell application"). The Applicant submits that the amended claim 1 is novel in view of the Honeywell application as the Honeywell application does not recite all of the relevant limitations of this claim. Before considering the limitations of claim 1, a review of the Honeywell application is necessary.

Firstly, it is important to understand the purpose of the Honeywell design - to reject "spurious" signals. The term "spurious" appears in the Abstract, each of the 21 claims, and repeatedly in the specification. "Spurious" signals are defined by Honeywell on page 1 at lines 26 - 32, and again on page 6 at lines 17 - 26 with respect to a specific example: when a 90MHz LO signal is used to demodulate a desired 80MHz signal, and there is a 100MHz "spurious" signal in the signal path, then both the desired signal and the spurious signal will demodulate to 10MHz. They explain that it is generally impossible to separate these two signals as they will overlap one another at 10MHz.

Honeywell proposes a two-stage mixing topology that demodulates the desired signal, but suppresses this spurious signal. They do this by using two local oscillators (LO) that one would see in a typical superheterodyne topology, except that the two LO signals are modulated with the same spread spectrum (SS) pattern before they mix with the input signal.

They argue that the desired 80MHz signal will be encoded by the first SS LO, and then decoded by the second. They also argue that the 100MHz will not be properly decoded by the second SS LO, so this signal would simply remain as noise at the output (lines 20 - 21 of page 6 read: "In other words, the desired signal is correctly spread in the bandwidth but the undesired signal is not." At lines 25 - 26 of page 6, Honeywell then notes: "... the desired signal may be recovered since it is spread differently from the undesired signal.")

Honeywell does not explain how or why this works, but they clearly argue that this topology will not modulate or demodulate all input signals - only the desired input signal. Note that the filter plays no part in this selection process, as in the example they present, the intermediate frequency (IF) of both the 80MHz and 100MHz inputs will be the same - 10MHz.

Looking now at the amended claim 1, we see the limitation at lines 3 - 4 that "$\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated",

and at lines 10 - 11 that the second mixer will "generate an output signal $x(t)\ \varphi_1\ \varphi_2$". Clearly, Honeywell is arguing that their modulation/demodulation topology does not satisfy either of these requirements, otherwise both the 80MHz and 100MHz signals would be demodulated equally, down to 1MHz at the output. That is:

- the claim requires the output to be equal to $x(t)\ \varphi_1\ \varphi_2$;
- given inputs of 80MHz and 100MHz, and SS LO signals of 90MHz of 9MHz, what is the output of the Honeywell topology?
- according to the Honeywell document, the 80MHz will be demodulated to 1MHz, but the 100MHz signal will not;
- however, if the output of the Honeywell topology was equal to $x(t)\ \varphi_1\ \varphi_2$, then it would demodulate both the 80MHz and 100MHz signals down to 1MHz, overlapping one another;
- it does not, thus, the Honeywell application does not anticipate the limitations of claim 1

Therefore, claim 1 is in compliance with the requirements of PCT Article 33(1), (2).

The Applicant also notes that because Honeywell is attempting to address a different problem than that of the invention (i.e. rejecting spurious input signals), that the skilled technician would not consider the Honeywell application in addressing the problems of the invention.

Also under item V. 2., the Examiner submitted that a typical superheterodyne topology also anticipates claim 1, as any LO signal produces a "time-varying" signal. While the Applicant feels that the meaning of the term "time-varying" is clear from a reading of the patent specification as a whole, he has amended this wording to "which vary irregularly over time", to make the distinction more clear. As noted above, this wording has basis in the specification at lines 15 - 18 of page 6.

The Applicant therefore asks that the Examiner withdraw this objection under PCT Article 33(1), (2).

Under item V. 3., the Examiner submitted that because claim 31 (the amended claim 30) generally corresponds to the same scope as claim 1, it similarly lacks novelty in view of reference D1. The Applicant notes that the same amendments and arguments noted above with respect to claim 1, apply equally to claim 31. The Applicant therefore submits that claim 31 is in compliance with the requirements of PCT Article 33(1), (2), and asks that the Examiner withdraw this objection.

Under item V. 4., the Examiner submitted that the balance of the claims are obvious in view of various prior references. The Applicant notes that all of these claims incorporate the limitations of claim 1. As presented above, claim 1 is novel and non-obvious in view of the cited references, therefore, the Applicant submits that each claim reciting at least the same limitations would similarly be novel and non-obvious.

Therefore, the Application asks that the Examiner withdraw this objection under PCT Article 33(3).

With regard to item VII. 1., Applicant submits that the inclusion of reference numbers in the claims is not entirely appropriate as the figures do not correspond precisely with the elements of the claims. The Applicant submits that it would be confusing to make reference to the figures as requested.

With regard to item VII. 2., Applicant wishes to defer the amendment of the Background to the Invention until national entry applications have been filed.

The Applicant submits that he has complied with the requirements of item VII. 3., noting that the basis for the amendments to the claims is provided above.

With regard to item VIII. 1., the Applicant disagrees with the Examiner, submitting that the scope of claim 1 would be clear to one skilled in the art. As noted in Article 6, II-4.2 of the PCT Guidelines: "The claim should also be read with an attempt to make technical sense out of it".

With regard to item VIII. 2., the Applicant again disagrees with the Examiner, as the scope of claim 2 would also be clear to one skilled in the art. While an input signal $x(t)$ may include spurious signals, noise, etc., it would be clear to the reader that an up-convertor would be designed with a particular purpose in mind, and that part of this design process would be the specification of the input and output signals involved.

The Applicant therefore asks that the Examiner withdraw these objections under PCT Article 6.

The Applicant believes that all of the objections levelled by the Examiner have now been addressed. The Applicant would be pleased to discuss any outstanding or new issues which may arise during preparation of a second Written Opinion, or the International Preliminary Examination Report.

for T. Gary O'Neill
Agent for the Applicant
TGO:MKL

114685.1

components **142**, **144** and **146** of **Figure 8** respectively, though their input signals are slightly different.

It is preferred to generate the inputs to the two mixers **142** and **144** by means of signal generation blocks **148** and **150**; signal generation block **148** generating the φ_1 signal and signal generation block **150** generating the φ_2 signal. Implementing the invention with separate I and Q channels would require four mixers, two per channel, and four φ signals; specifically, φ_1I and φ_1Q; and φ_2I and φ_2Q, as shown in **Figure 6**.

The input to these generation blocks **148** and **150** is an oscillator which does not have a significant amount of signal power at the frequency of the desired output RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 5**. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. PCT/CA00/00996.

The embodiment of **Figure 8** is distinct from that of **Figure 7** with regard to the feedback control loop. Power measurement of the RF output signal is performed by the power measurement unit **152**, but rather than optimising for $\frac{dP_M}{d(delay)} = 0$ as per the embodiment presented in **Figure 7**, the control loop is optimised for $\frac{dP_M}{d(DCoffset)} = 0$ using detector **154**, which drives the DC offset generator **156**.

DC offset is affected in the baseband signal by means of the summer **158** which sums the input baseband signal with the direct current offset from the DC offset generator **156**. Suitable components for the DC offset generator **156** and summer **158** are known in the art.

The physical order (that is, arrangement) of the BPF **146**, the DC offset correction summer **158**, and any additional gain control elements (none shown) can be rearranged to some degree. Such modifications would be clear to one skilled in the art.

COMPARE DOCUMENT

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said ~~time-varying~~mixing signal φ_1 to generate an output signal *x(t)* φ_1; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal *x(t)* φ_1 with said ~~time-varying~~mixing signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal *x(t)* φ_1 φ_2; and

a time-varying signal modification circuit for modifying a parameter of one of said ~~time-varying~~mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where said ~~time-varying~~mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, ~~further comprising~~where said filter comprises:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying signals are irregular~~synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:

a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal *x(t)* φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said ~~time-varying~~mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, ~~further comprising:~~

~~a filter for removing unwanted signal components.~~

~~30. The radio frequency (RF) up-convertor of claim 1, further comprising:~~

~~a filter for removing unwanted signal components from said *x(t)* φ_1 signal.~~

~~31~~where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

30. A method of modulating a baseband signal *x(t)* comprising the steps of:

generating ~~time-varying~~mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal *x(t)* with said ~~time-varying~~mixing signal φ_1 to generate an output signal *x(t)* φ_1; and

mixing said signal *x(t)* φ_1 with said ~~time-varying~~mixing signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

321. An integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - ~~30~~29.

332. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - ~~30~~29.

343. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - ~~30~~29.

NEW CLAIMS

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1\ \varphi_2$; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, where said filter comprises:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:
a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

30. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal $x(t)$ with said mixing signal φ_1 to generate an output signal $x(t)$ φ_1; and

mixing said signal $x(t)$ φ_1 with said mixing signal φ_2 to generate an output signal $x(t)$ φ_1 φ_2.

31. An integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

32. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

33. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

PATENT COOPERATION TREATY

From the:
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

HARRIS, J. et al.
Gowling Lafleur Henderson LLP
Suite 2600
160 Elgin Street
Ottawa, Ontario K1P 1C3
CANADA

PCT

WRITTEN OPINION

(PCT Rule 66)

Date of mailing *(day/month/year)*	17.07.2001
Applicant's or agent's file reference: O8-887953WO	**REPLY DUE** **within 3 month(s)** from the above date of mailing

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA00/00995	01/09/2000	01/09/1999

International Patent Classification (IPC) or both national classification and IPC
H04B1/04

Applicant
SiRiFIC WIRELESS CORPORATION

1. This written opinion is the **first** drawn up by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

I	☒	Basis of the opinion
II	☐	Priority
III	☐	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	☐	Lack of unity of invention
V	☒	Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
VI	☐	Certain document cited
VII	☒	Certain defects in the international application
VIII	☒	Certain observations on the international application

3. The applicant is hereby **invited to reply** to this opinion.

When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(d).

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also: For an additional opportunity to submit amendments, see Rule 66.4.
For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 bis.
For an informal communication with the examiner, see Rule 66.6.

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 01/01/2002.

Name and mailing address of the international preliminary examining authority:
European Patent Office
D-80298 Munich
Tel. +49 89 2399 - 0 Tx: 523656 epmu d
Fax: +49 89 2399 - 4465

Authorized officer / Examiner
Kolbe, W

Formalities officer (incl. extension of time limits)
Kiepe, C
Telephone No. +49 89 2399 2423

I. Basis of the opinion

1. With regard to the **elements** of the international application (Replacement *sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed"*):

Description, pages:

1-15 as originally filed

Claims, No.:

1-34 as originally filed

Drawings, sheets:

1/10-10/10 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1,31
Inventive step (IS)	Claims	2-30,32-34
Industrial applicability (IA)	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:

   D1: WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11)
   D2: EP-A-0 899 868 (MITEL CORP) 3 March 1999 (1999-03-03)

2. Document D1, see in particular the passages cited in the search report, discloses as in claim 1:

   A radio frequency (RF) up-convertor with reduced local oscillator leakage for modulating an input signal x(t)(i.e. 80 MHz, D1 clearly discloses that the convertor can be used for transmission conversion, see claim 11 and page 7 line 12, this implies an up-conversion, although the frequencies refer to the embodiment of Figure 2 which relates to a down-conversion), comprising:
   a synthesizer for generating time-varying signals φ1 and φ2; where φ1*φ2 has significant power at the frequency (i.e. 81 MHz) of the local oscillator being emulated, and neither φ1 nor φ2 has significant power at the frequency of said local oscillator being emulated

   a first mixer (21) coupled to said synthesizer for mixing said input signal x(t) with said time varying signal φ1 to generate an output signal x(t) φ1; and

   a second mixer (26) coupled to said synthesizer and to the output of said first mixer for mixing said signal x(t) φ1 with said time varying signal φ2 to generate an output signal x(t) φ1 φ2

   The references in parentheses apply to the figures of D1.

   Since all the features of claim 1 are known from D1, the claim lacks novelty in the sense of Article 33(1),(2) PCT.

It should be noted that any two stage mixer falls into the scope of claim 1, since every local oscillator produces a "time-varying signal" because the voltage of such a signal varies in time with the frequency of the oscillator. The two conventional local oscillators of a double-superheterodyne stage emulate what the present application calls a "virtual local oscillator" whereby the sum or the difference of the frequencies of the two conventional local oscillators is considered the frequency of the "virtual local oscillator".

3. The subject-matter of independent claim 31 corresponds to the subject-matter of claim 1, hence the above argumentation correspondingly applies to independent method claim 31.

4. Dependent claims 2 to 30 and 32 to 34 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, involve an inventive step (Article 33(3) PCT) since these claims merely define an association of known features (see also D2 to D4) functioning in their normal way and, in combination, not producing any non-obvious working interrelationship, cf. PCT Guidelines Chapt. IV,8.8(B1).

Re Item VII
Certain defects in the international application

1. The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

2. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D2 is not mentioned in the description, nor are these documents identified therein.

3. If an amended set of claims is filed, then the description has to be adapted accordingly. The applicant is further requested to provide clear indication from where in the original application the amendments were derived, cf. Article 19(2) PCT.

Re Item VIII

Certain observations on the international application

1. Claim 1 tries to define the up-converter using parameters (the power at the frequency of a local oscillator being emulated) which are unsuitable to clearly define the structure of the up-convertor to be protected. Claim 1 is thus unclear in the sense of Article 6 PCT.

2. Claim 2 tries to define the convertor by reference to the input signal x(t) which may be applied to the a mixer of the convertor. Such a definition is unsuitable to clearly define the structure of the claimed convertor. This claims is thus unclear, Article 6 PCT.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
08-887953WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/CA 00/ 00995	01/09/2000	01/09/1999
Applicant		
SiRiFIC WIRELESS CORPORATION		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 5

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
CA 00/00995

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/04 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11) abstract page 2, line 1 - line 16 page 4, line 5 - line 22 claims 1-7; figure 2	1-3, 20-24, 29-31
X	EP 0 899 868 A (MITEL CORP) 3 March 1999 (1999-03-03) abstract column 1, line 22 - line 42 claims 1-6	1,20,21, 31

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2001	24/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Lazaridis, P

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
CA 00/00995

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9601006 A	11-01-1996	AU 2909795 A	25-01-1996
EP 0899868 A	03-03-1999	CA 2245958 A	28-02-1999